Date @qualcomm Location

Qualcomm

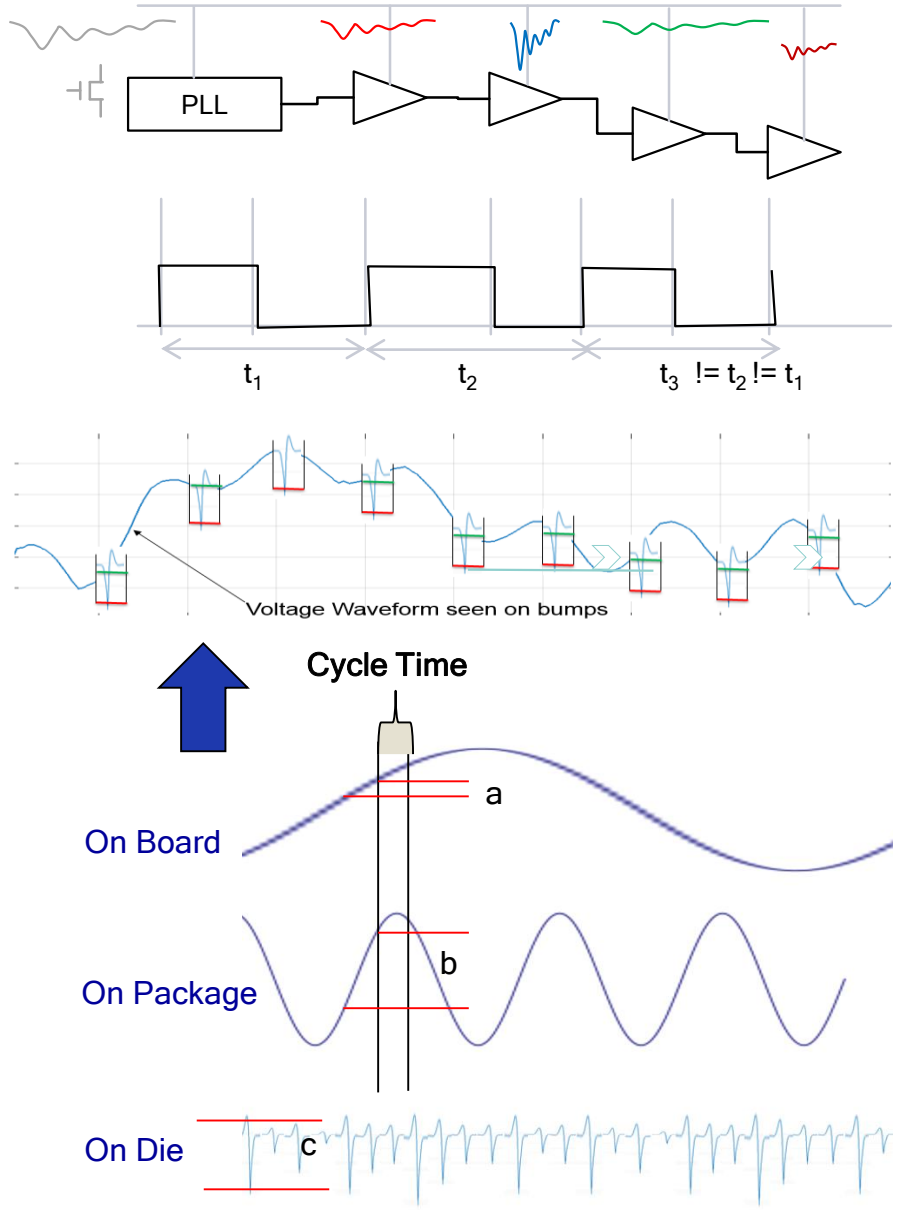
CTS Jitter: Analysis and Robustness Against Power Supply Noise

Palkesh Jain (Principal Engineer), Mahesh Yatagiri (Sr. Lead Engineer), Dawuth Pathan (Sr. Engineer), Ashwath Prabhu (Engineer)

Qualcomm India Pvt Ltd.
email: palkesh@qti.qualcomm.com

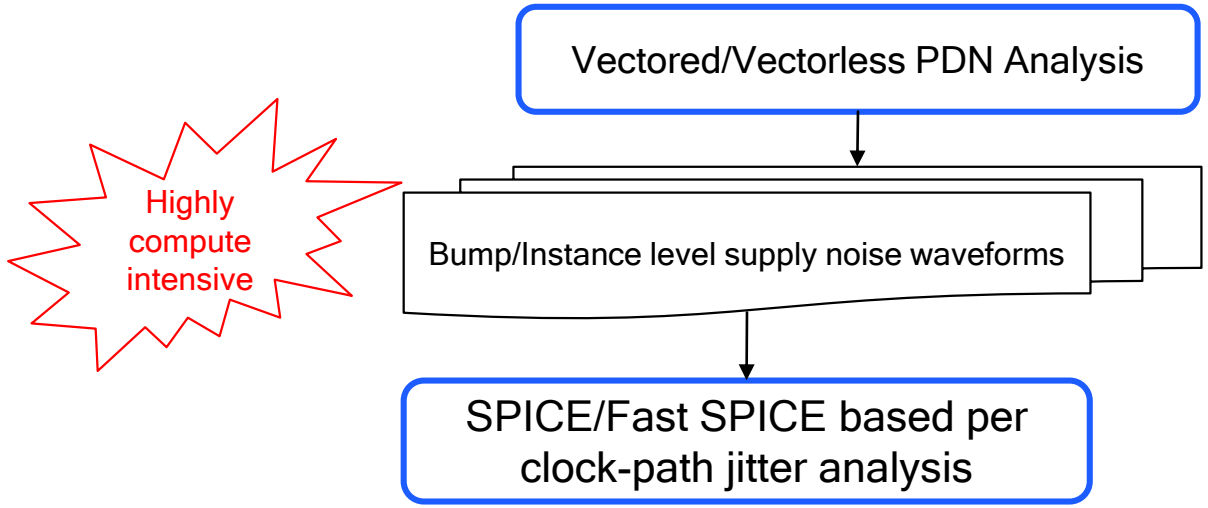
CTS Jitter: Genesis

- Jitter : Clock network delay uncertainty; from one clock cycle to the another. Primarily driven by power supply noise variations, temperature variations and random variations (Lg, Gox).
  - PLL Jitter: accumulation due to the integrator in the feedback loop.
  - CTS Jitter: Depends on cycle-to-cycle variations in the voltage seen on the instances. Interest of this work.
- Voltage seen on an instance has 3 components:
  - Low frequency (board induced)
  - Mid frequency (package induced)
  - High frequency (on-die)



Existing Largescale Frameworks and Shortcomings

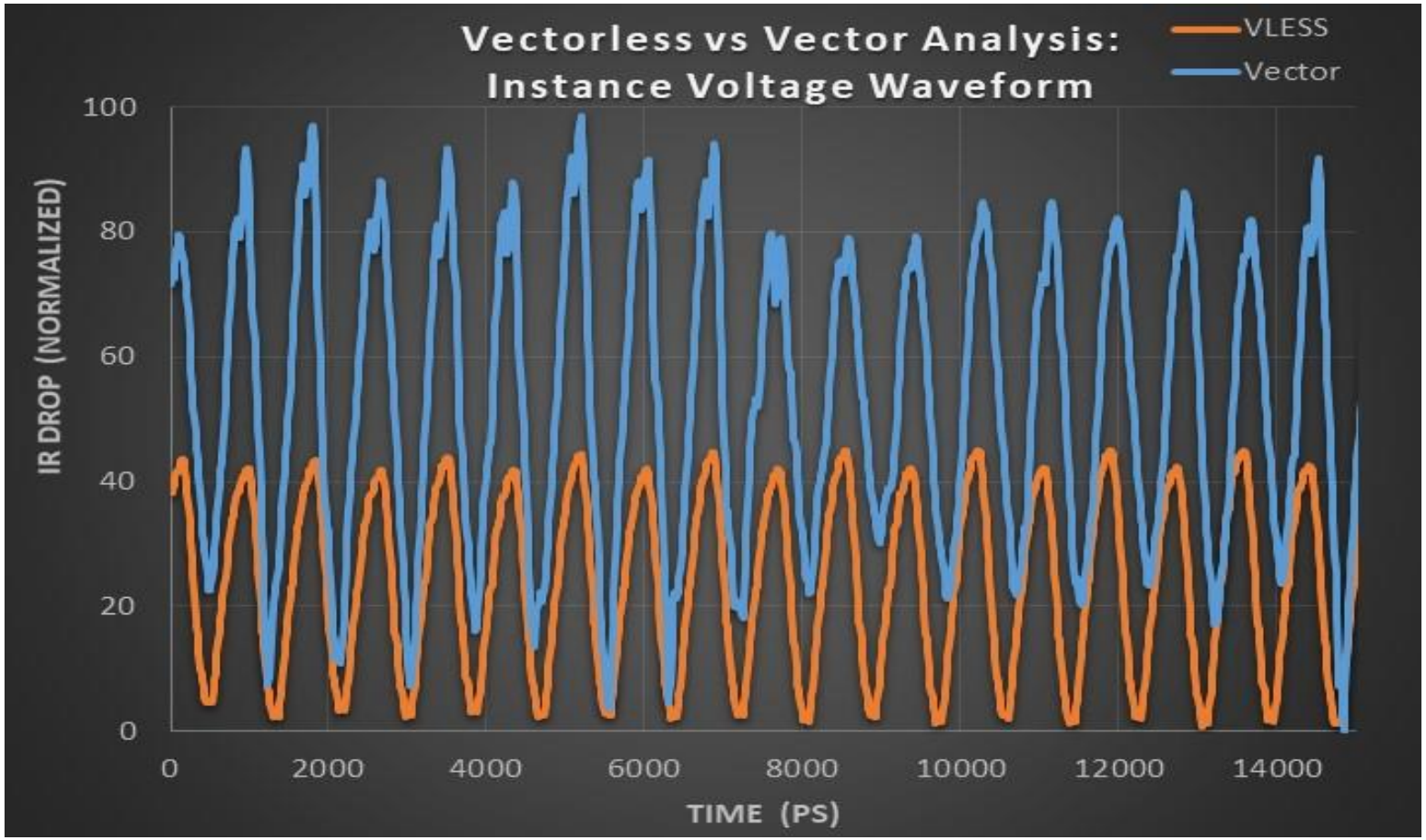
- Some of the existing large scale frameworks rely on two-step method:
  - Brute force voltage noise estimation on clock instances
  - SPICE driven voltage-to-jitter impact estimation after simulating the clock tree



- Few limitations of the existing flows:
  - Extremely resource intensive, considering multiple PVTs and modes.
  - Often, turns into a single margin number which gets applied to all variety of clocks, or is often available very late in the design cycle.
  - Strongly coupled to the noise analysis methodology and IR drop simulations.

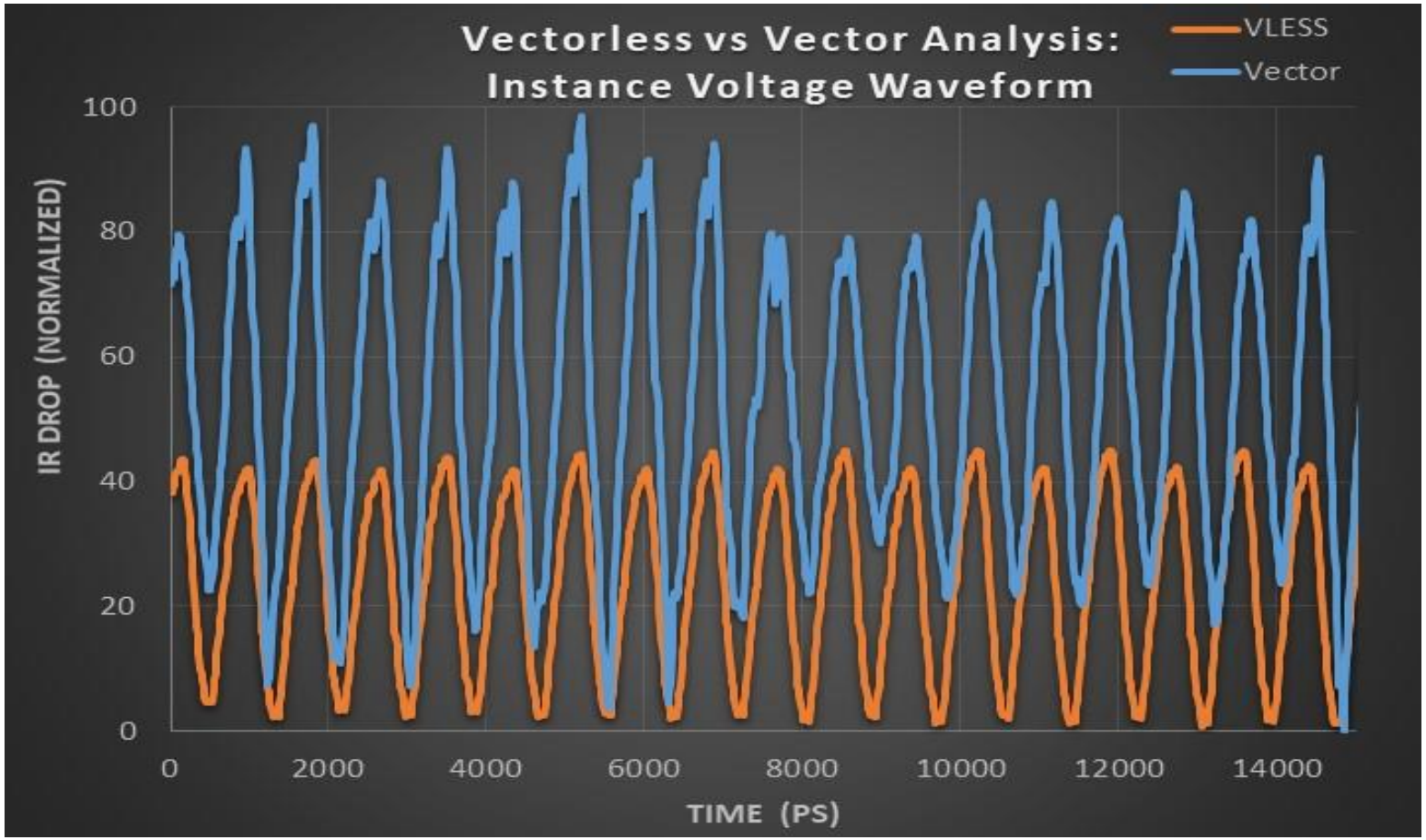
Vectorless vs Vectored-Noise based Jitter Analysis

- Vectorless noise estimation primarily assesses high frequency (localized) switching.
- However, it runs the risk of
  - exciting same instances in every cycle : very low HF C2C, or,
  - a completely uncoherent switching scenario



Vectorless vs Vectored-Noise based Jitter Analysis

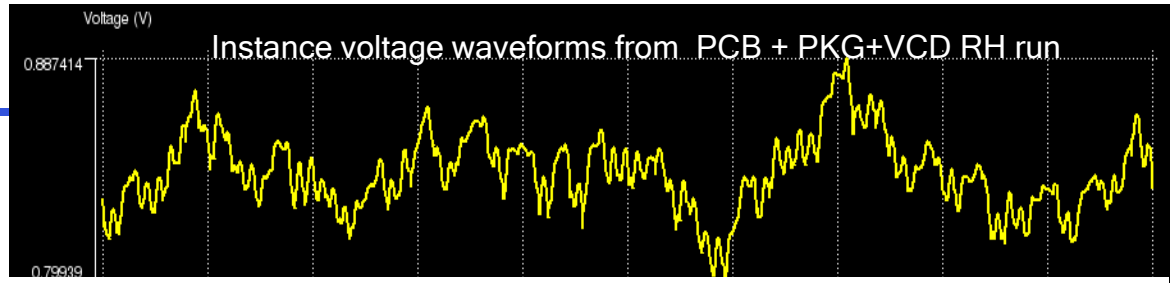
- Vectorless noise estimation primarily assesses high frequency (localized) switching.
- However, it runs the risk of
  - exciting same instances in every cycle : very low HF C2C, or,
  - a completely uncoherent switching scenario



- On the other hand, vector based simulation can potentially show realistic C2C variations (depending on the topology and other design details)

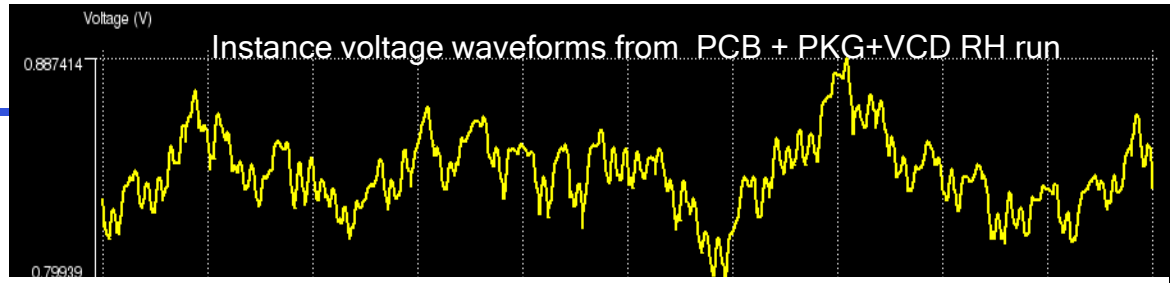
Noise-Frequency Impact on Jitter

- To further breakdown the jitter estimations from vectorless and VCD simulations, we study the individual noise spectra resulting from these simulations.

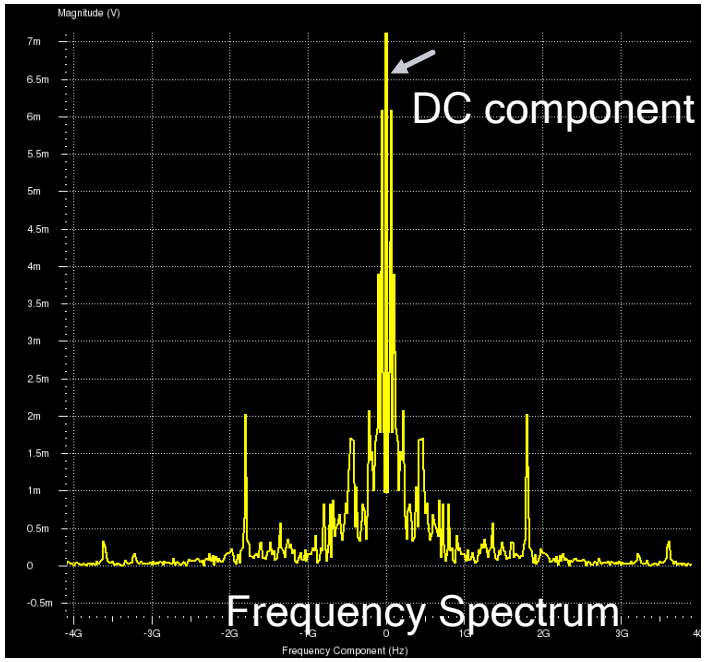


- For every instance on the clock path:
  - We estimate the effective voltage waveform (Vdd – Vss).

Noise-Frequency Impact on Jitter



- To further breakdown the jitter estimations from vectorless and VCD simulations, we study the individual noise spectra resulting from these simulations.

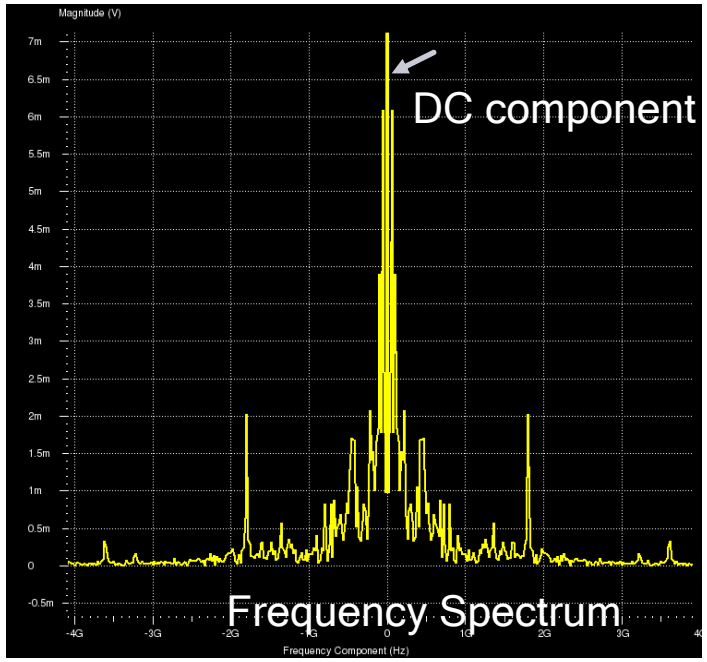


Frequency spectrum for the noise waveforms

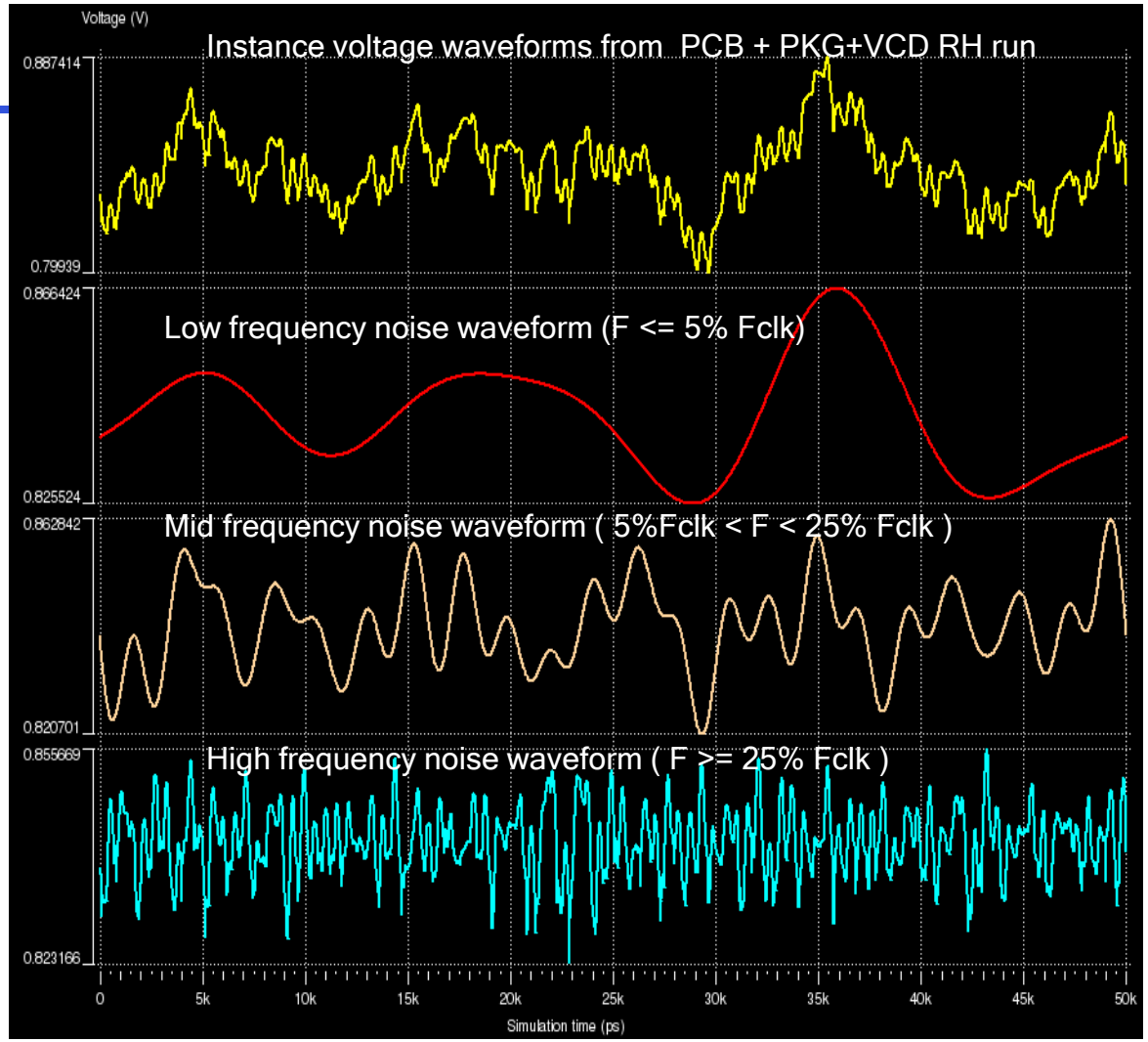
- For every instance on the clock path:
  - We estimate the effective voltage waveform (Vdd – Vss).
  - Perform FFT on the voltage waveform to get the frequency spectrum.

Noise-Frequency Impact on Jitter

- To further breakdown the jitter estimations from vectorless and VCD simulations, we study the individual noise spectra resulting from these simulations.



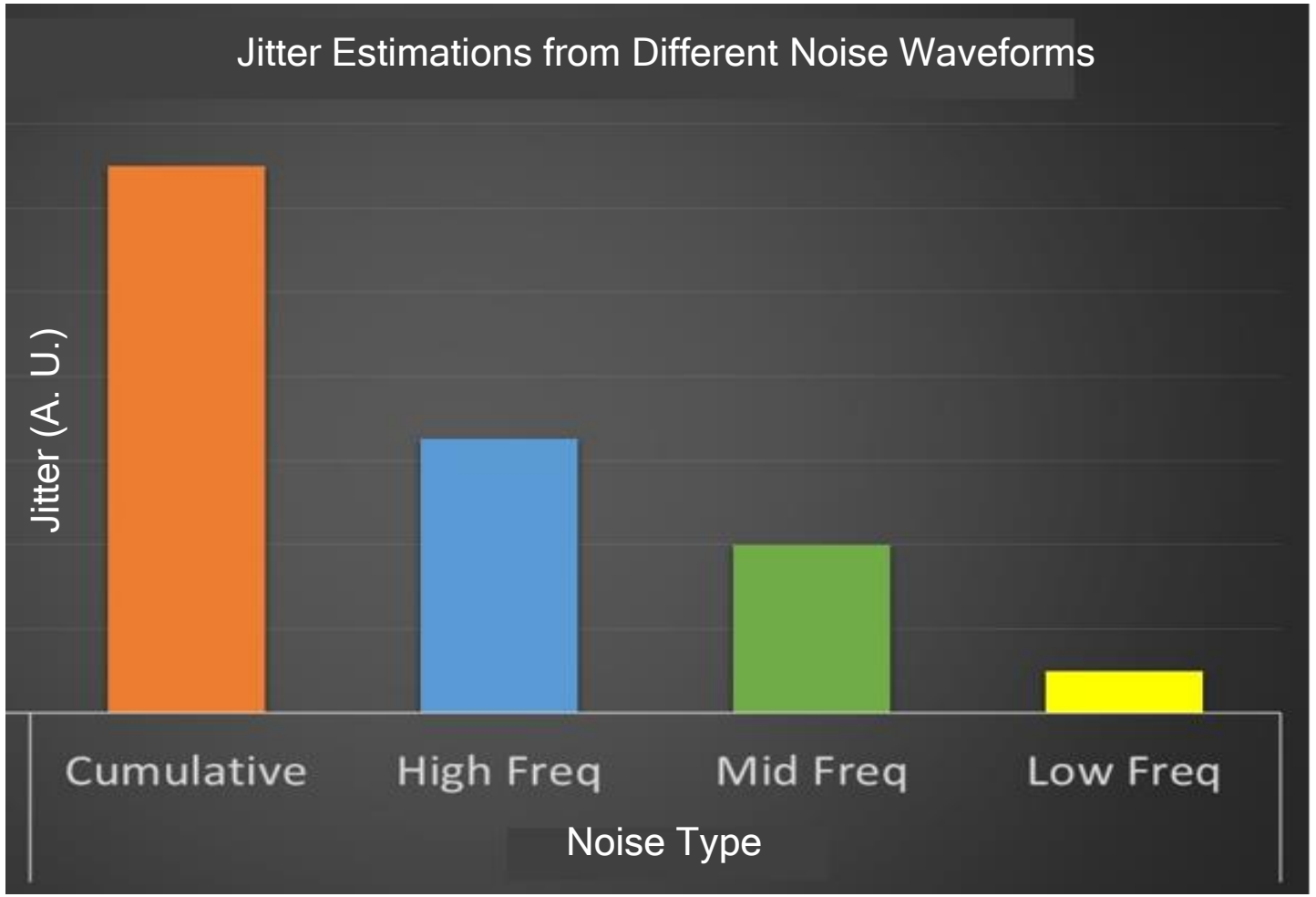
Frequency spectrum for the noise waveforms



- For every instance on the clock path:
  - We estimate the effective voltage waveform (Vdd – Vss).
  - Perform FFT on the voltage waveform to get the frequency spectrum.
  - Choose the low/band/high-pass frequency bands as (0-5%Fmax), (5%-25%Fmax) and (25%Fmax -).
  - Reconstruct the waveform in those bands to get 3 different noise waveforms, corresponding to the low/band/high freq. noises.

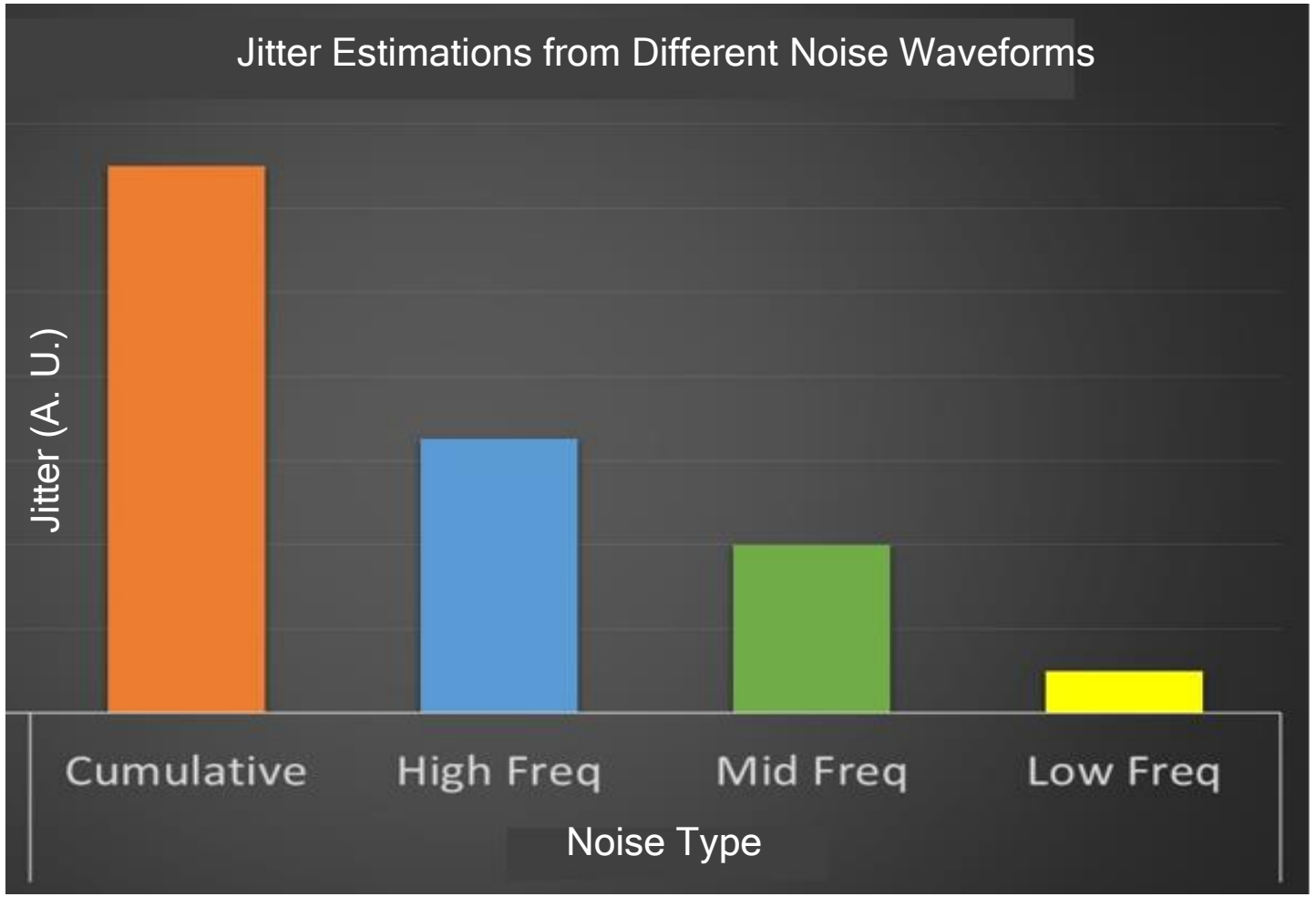
Noise-Frequency Impact on Jitter

- We perform SPICE based clock-tree jitter estimation using various noise waveforms:
  - Full (cumulative; untampered)
  - Low frequency noise
  - Mid frequency noise
  - High frequency noise



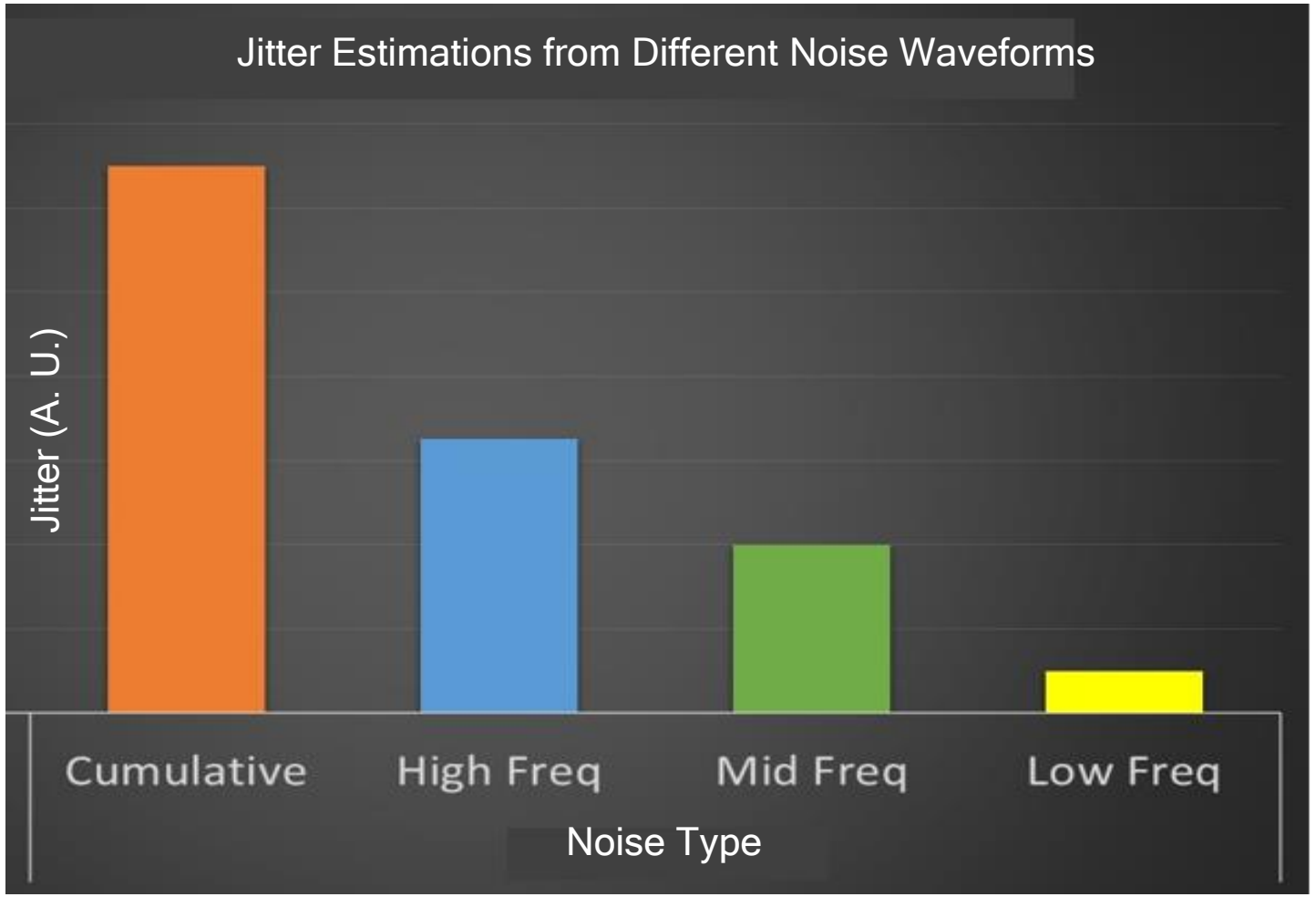
Noise-Frequency Impact on Jitter

- We perform SPICE based clock-tree jitter estimation using various noise waveforms:
  - Full (cumulative; untampered)
  - Low frequency noise
  - Mid frequency noise
  - High frequency noise
- Our observations clearly indicate: :
  - Low freq. noise creates minimal jitter
  - High frequency noise is a large contributor



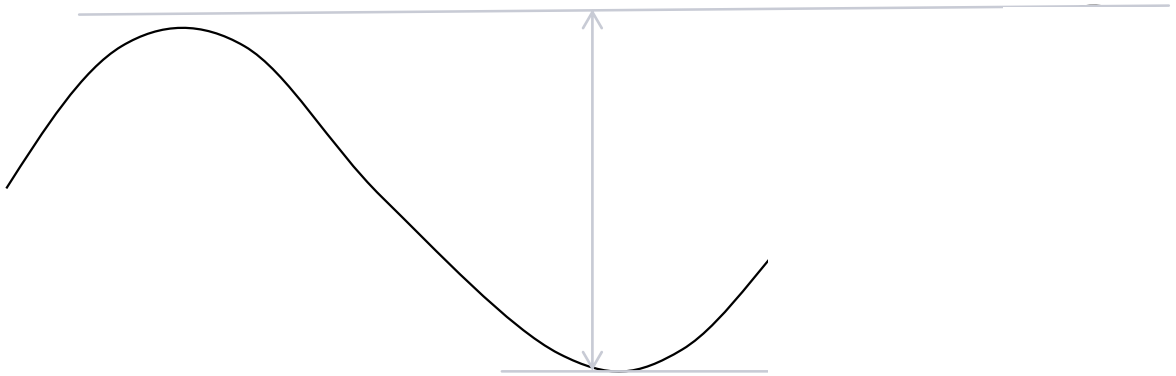
Noise-Frequency Impact on Jitter

- We perform SPICE based clock-tree jitter estimation using various noise waveforms:
  - Full (cumulative; untampered)
  - Low frequency noise
  - Mid frequency noise
  - High frequency noise
- Our observations clearly indicate: :
  - Low freq. noise creates minimal jitter
  - High frequency noise is a large contributor



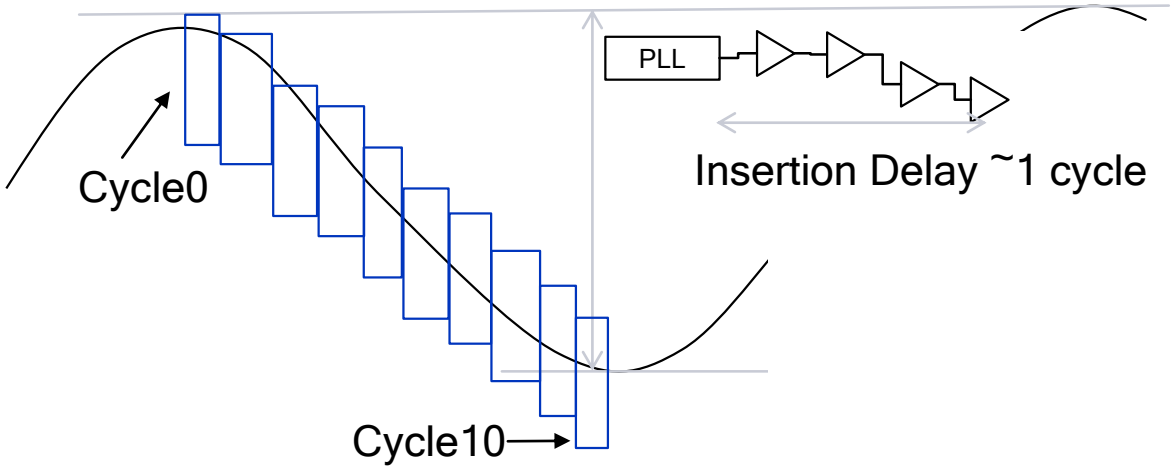
So, we now explore methodologies which can help understand low frequency and high frequency noises separately in a more scalable and easier framework

Low Frequency Analysis (F < 5% F_{clk})



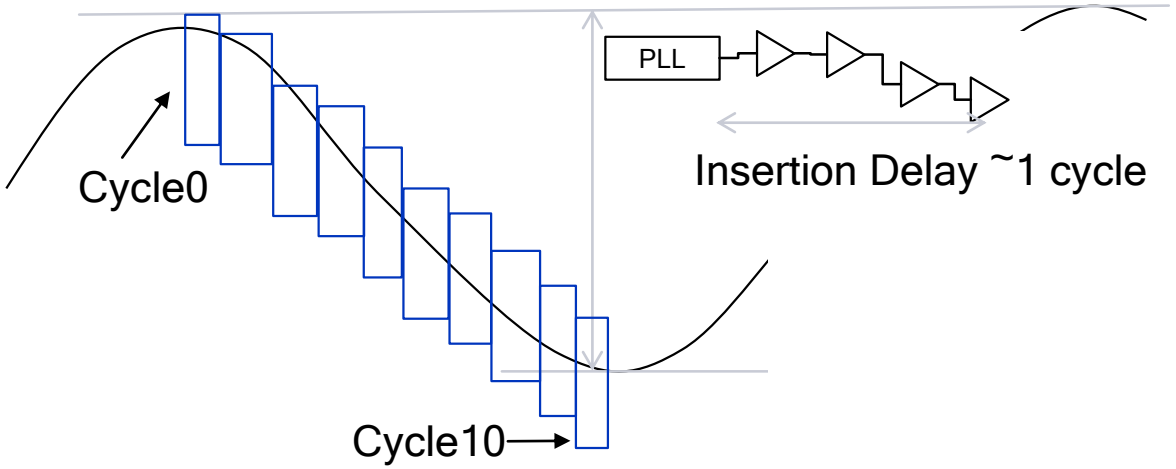
- Typical low frequency noises in the range of 5% F_{clk}

Low Frequency Analysis (F < 5% F_{clk})



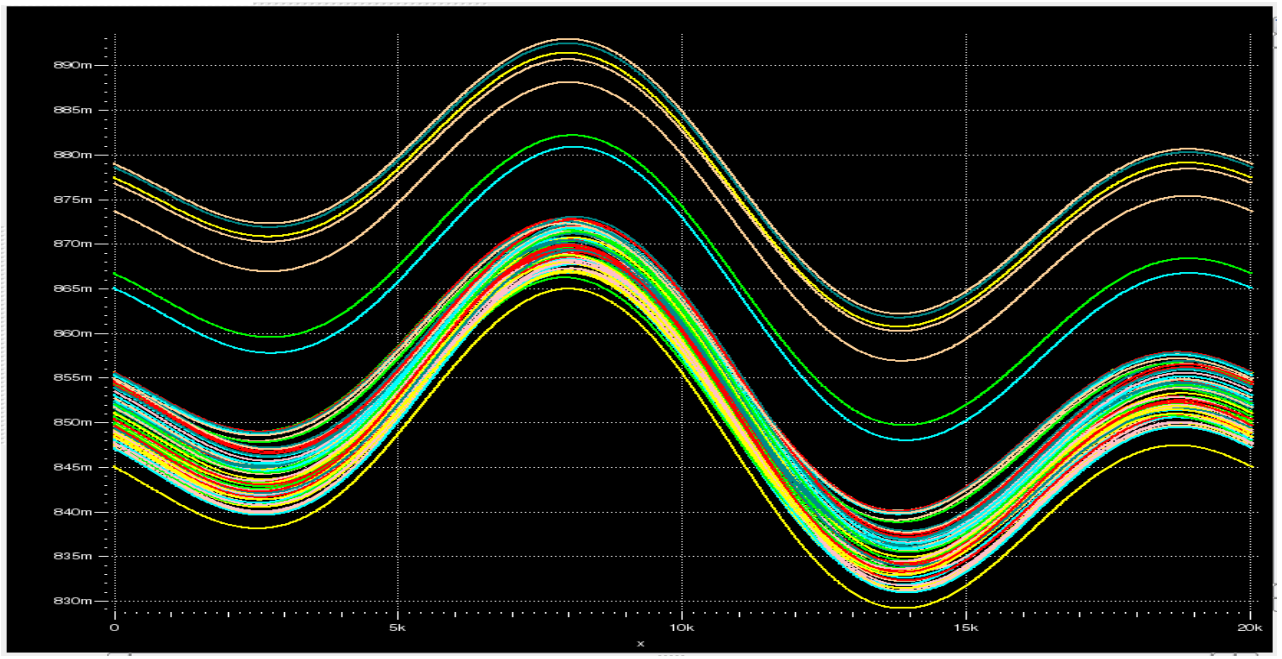
- Typical low frequency noises in the range of 5% F_{clk}
- Considering the insertion delays ~ 1cycle for high perf. designs, overall, low frequency noises are expected to cause low jitter

Low Frequency Analysis (F < 5% F_{clk})

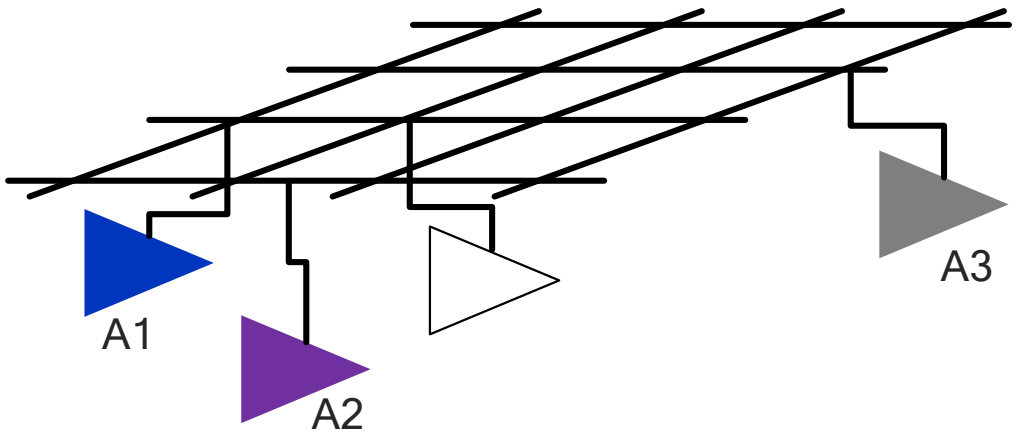


- Typical low frequency noises in the range of 5% F_{clk}
- Considering the insertion delays ~ 1cycle for high perf. designs, overall, low frequency noises are expected to cause low jitter

- Additionally, considering the global nature of the low frequency noise, there is only a marginal instance-to-instance variation in the low frequency noise

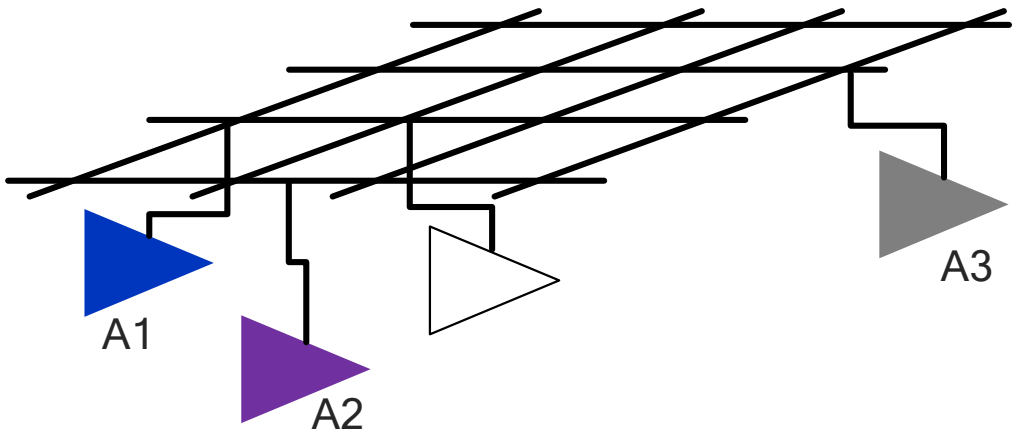


High Frequency Drop – Deeper Look

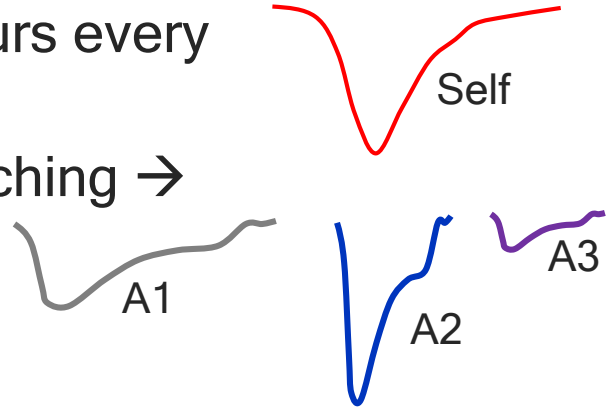


- Drop on the CTB can be categorized as:
  - Self-switching induced → occurs every cycle; very regular.

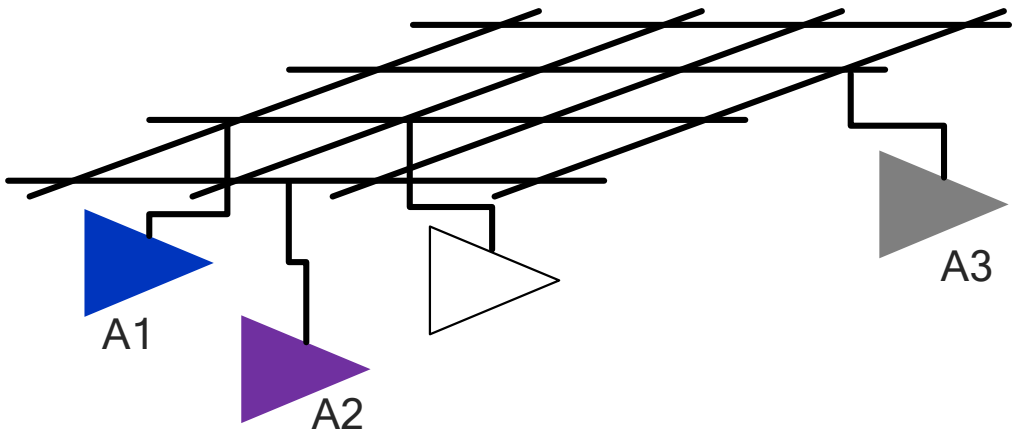
High Frequency Drop – Deeper Look



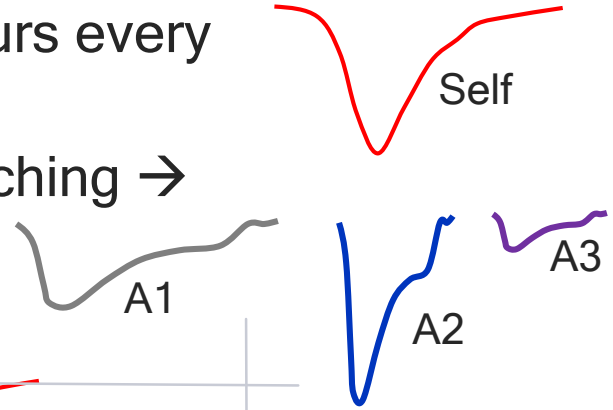
- Drop on the CTB can be categorized as:
  - Self-switching induced → occurs every cycle; very regular.
  - Neighborhood/Aggressor switching → causes irregular noise on the victim CTB



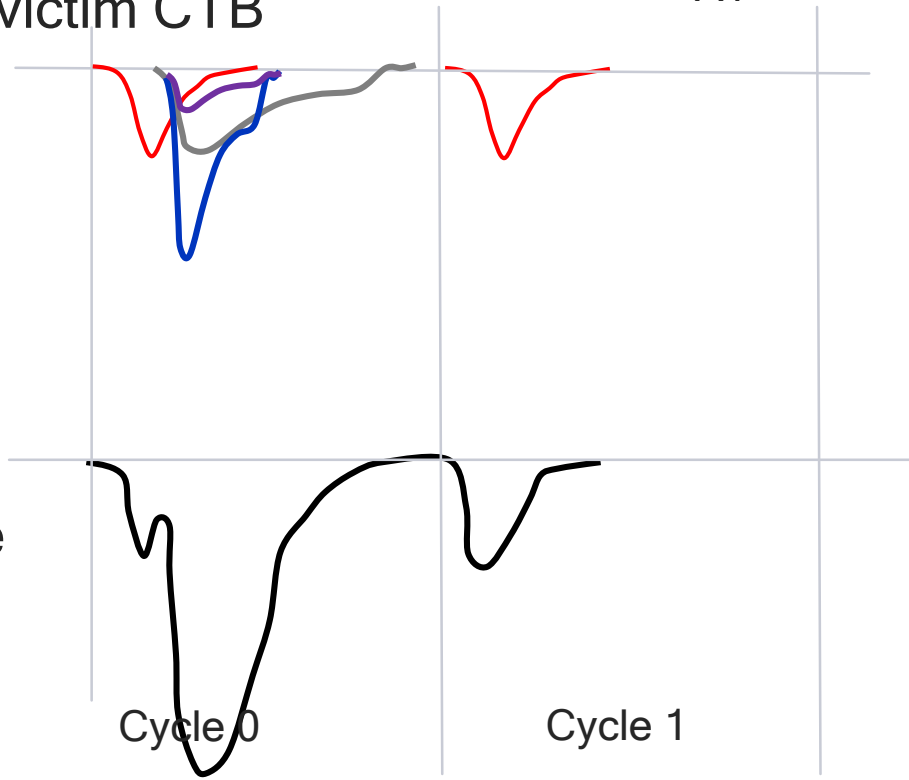
High Frequency Drop – Deeper Look



- Drop on the CTB can be categorized as:
  - Self-switching induced → occurs every cycle; very regular.
  - Neighborhood/Aggressor switching → causes irregular noise on the victim CTB

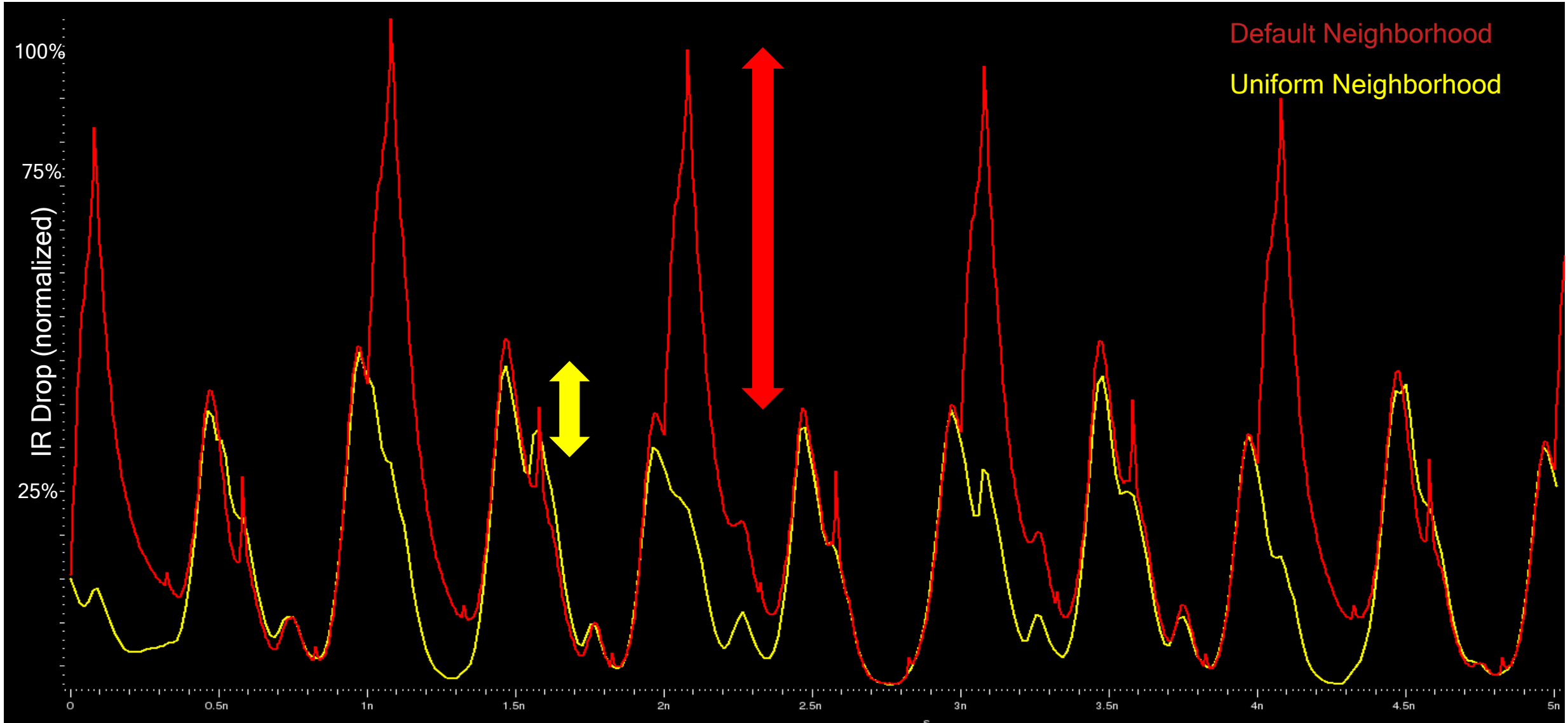


- Postulating that irregular neighborhood switching causes high frequency jitter:
  - we begin by tracing various clock paths in the design
  - identifying the aggressors for each buffer
  - predicting the drop on the buffer-under-test by the irregular neighborhood switching

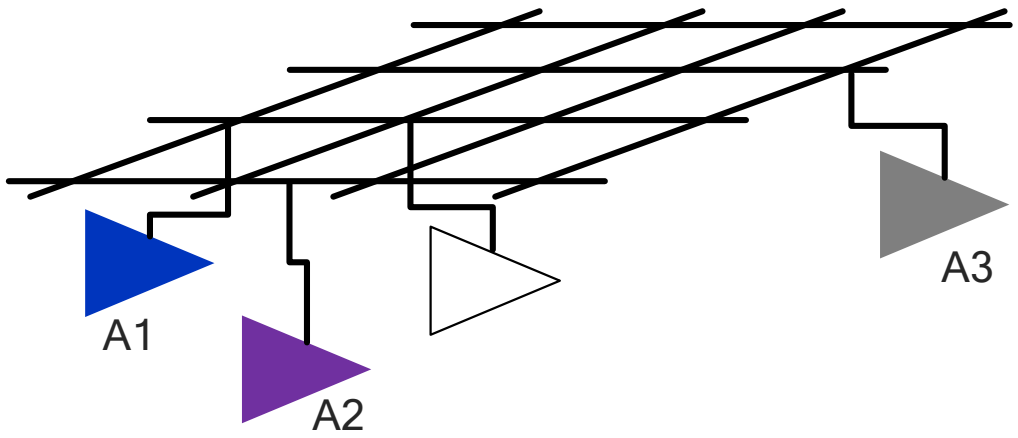


Neighborhood Impact on Jitter (through PDN simulations)

- Indeed, if the CTB neighbourhood is well controlled, we can observe significant improvement in C2C voltage variations; as seen in the graph below obtained from Redhawk simulations

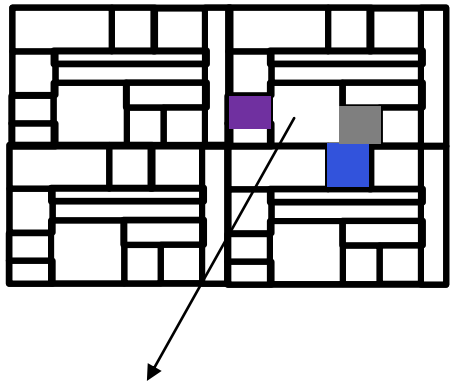


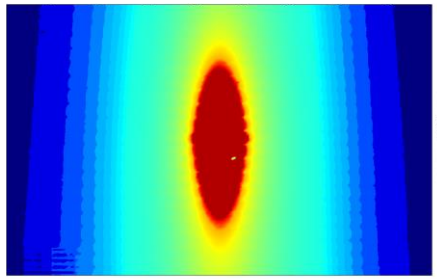
Neighborhood Impact Estimation



- While previous results were from the actual Redhawk simulations, we can analytically estimate the impact of neighborhood switching on a clock tree buffer.
  - Using principles of LTI and superposition

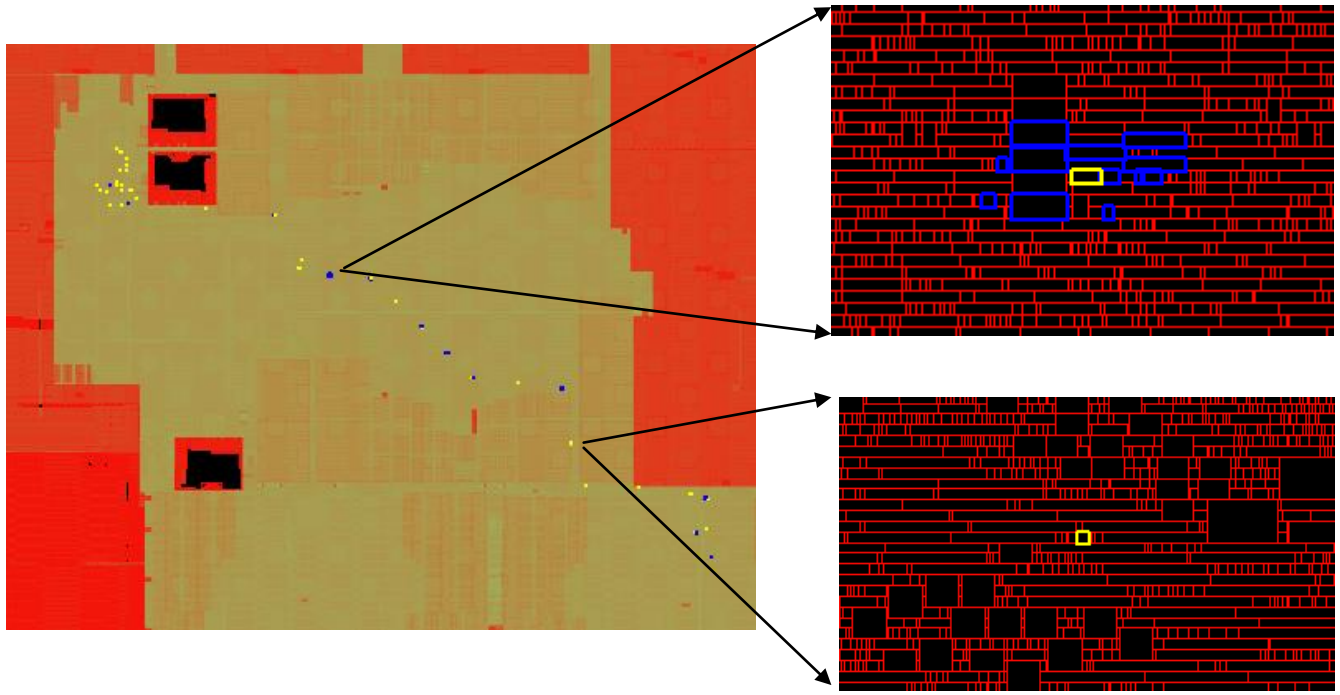
- We make use of the following characteristics in order to derive the instance impact
  - Relative placement of neighbors wrt clock tree buffer
  - Neighboring cell characteristics (timing window overlap)
  - IR drop due to unit current convoluted with the neighbor's switching current

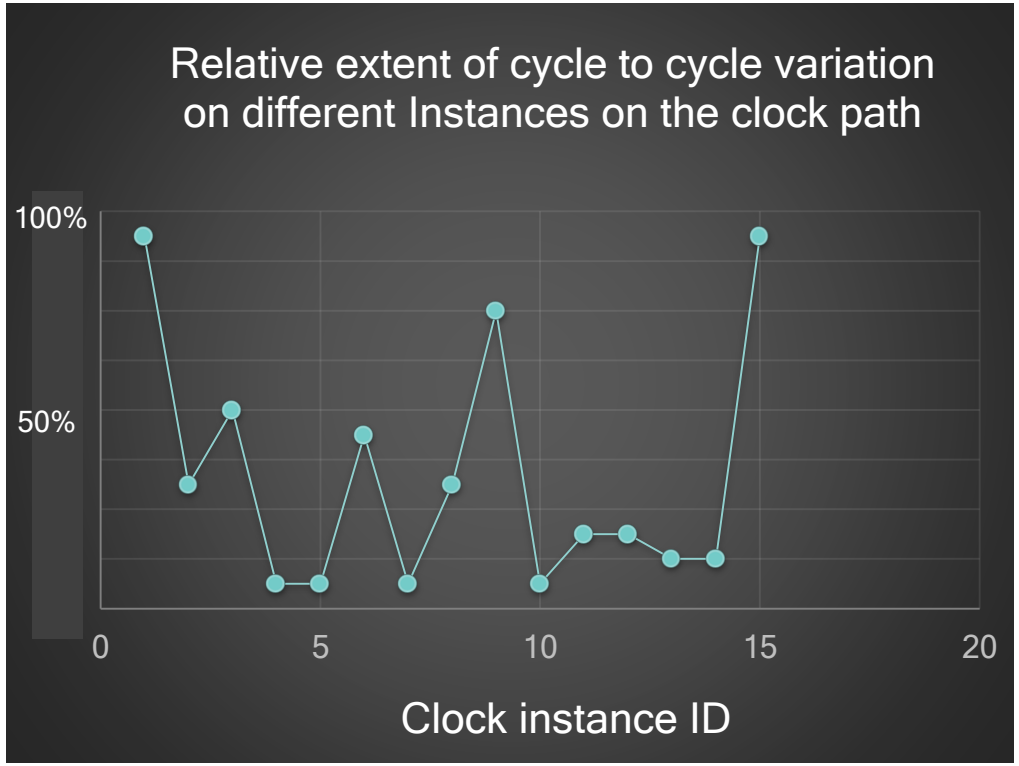

Instance under observation


Unit IR drop (normalized)

Structural Improvements from CTS Jitter Considerations

- Using the high frequency jitter impact framework, significant insights into structural weaknesses of the clock tree can be uncovered and fixed

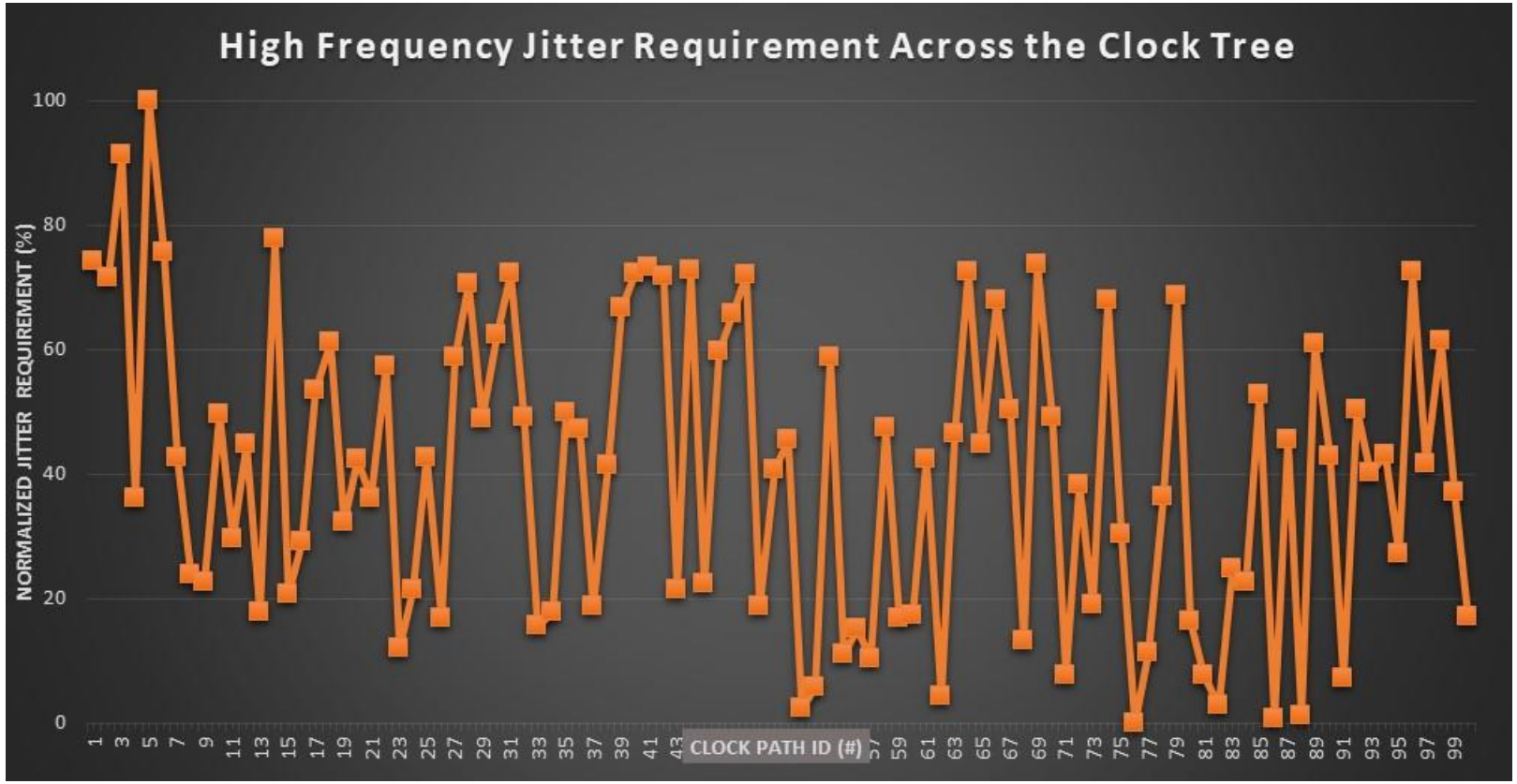




- As an example, in above case, CTB instances with varying extent of neighborhood impact can be highlighted and corrected through design actions

Results: High Frequency CTS Jitter from Several Clock Paths

- The developed methodology was run across all clock paths in the design for high frequency jitter estimation.
- From heuristics, the appropriate selection of the exact neighborhood switching was derived to finally estimate the jitter impact.
- Our observations are as follows:
  - High frequency jitter shows a significant variation (25 % - 100%) of max. jitter number.
  - Thus, a single jitter number cannot be used to margin all high frequency noises.



  - Some paths clearly have pathological reasons for high jitter (as highlighted through the structural assessment of the clock tree)

Conclusions

- CTS jitter directly impacts PPA in high performance modes. In this work, we systematically studied the jitter estimations from vectorless and vector-based supply noise waveforms. Our observations:
  - **Low frequency jitter impact is minimal** on high performance designs.
  - On the other hand, **high frequency jitter can be significant component**.

Conclusions

- CTS jitter directly impacts PPA in high performance modes. In this work, we systematically studied the jitter estimations from vectorless and vector-based supply noise waveforms. Our observations:
  - **Low frequency jitter impact is minimal** on high performance designs.
  - On the other hand, **high frequency jitter can be significant component**.

- For high frequency jitter estimates, we presented **a novel heuristics based fast and early analysis methodology**.
  - Our approach does not involve Redhawk computations and works in a ground up manner to identify the source of the high frequency jitter. The flow identifies the root cause, eventually resulting into high frequency jitter on clock path.
  - We analyze every single clock path and highlight the susceptible clock paths along with suggestions for improvements.

Conclusions

- CTS jitter directly impacts PPA in high performance modes. In this work, we systematically studied the jitter estimations from vectorless and vector-based supply noise waveforms. Our observations:
  - **Low frequency jitter impact is minimal** on high performance designs.
  - On the other hand, **high frequency jitter can be significant component**.

- For high frequency jitter estimates, we presented **a novel heuristics based fast and early analysis methodology**.
  - Our approach does not involve Redhawk computations and works in a ground up manner to identify the source of the high frequency jitter. The flow identifies the root cause, eventually resulting into high frequency jitter on clock path.
  - We analyze every single clock path and highlight the susceptible clock paths along with suggestions for improvements.

- Our estimates indicate a path specific high frequency jitter is warranted, **which cannot be accurately accounted through a single jitter number.**

Qualcomm

Thank you!

Follow us on:

For more information, visit us at:

www.qualcomm.com & www.qualcomm.com/blog